淡江大學 105 學年度日間部轉學生招生考試試題

系別：電機工程學系三年級　　科目：電　子　學

考試日期：7 月 22 日(星期五) 第 1 節　　本試題共 5 大題，2 頁

本試題雙面印刷

1. Design the circuit shown in Fig. 1, such that $I_C = 1.5mA$ and $V_C = 4V$, Assume $\beta = 100$. (20%)

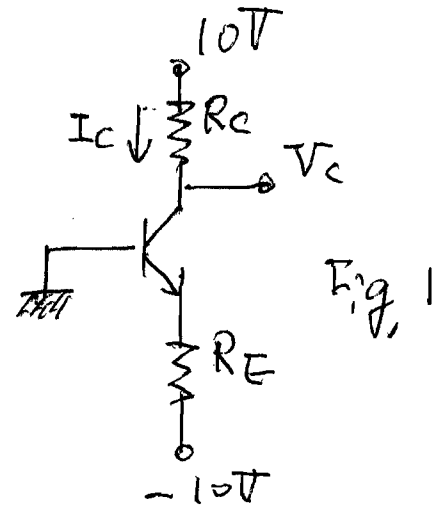

Fig. 1

2. The circuit of Fig 2 is a Two-input bipolar NOR logic circuit, where $V_{CE(sat)} = 0.2V$. Describe and verify the logic circuit response with truth table. (20%)

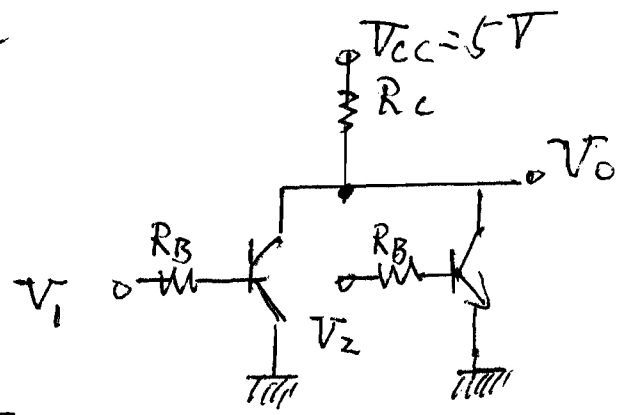

Fig. 2

3. Consider the circuit shown in Fig. 3, Determine I_B, I_C, I_E and V_{CE} for $\beta = 80$. Note: Assume the B-E cut-in voltage is 0.7V and C-E saturation voltage is 0.2V. (20%)

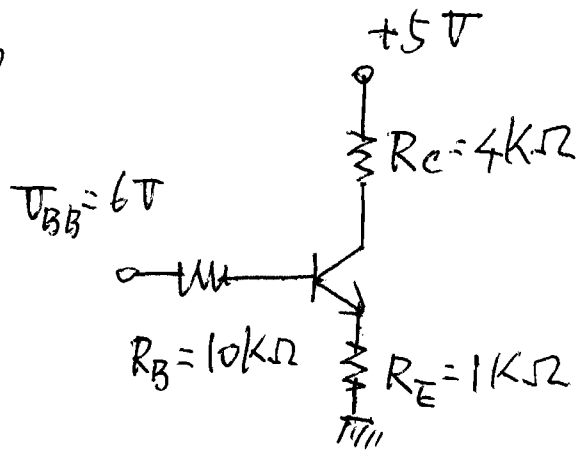

Fig. 3

背面尚有試題

淡江大學 105 學年度日間部轉學生招生考試試題

系別：電機工程學系三年級　　科目：電 子 學　　20-2

考試日期：7 月 22 日(星期五) 第 1 節　　本試題共 5 大題，2 頁

10%

4. (a) Explain the meaning of pinch off condition for a pn JFET.

(b) JFETs were developed before MOSFETs, but the applications and uses of the MOSFET have far surpassed those of the JFET, why ? 10%

5. Consider the circuit shown in Fig. 4. The transistor parameters are $V_{th}=0.2V$, $K=1.1mA/V^2$ and $\lambda=0$. Let $R_1+R_2=50K\Omega$. Design the circuit such that $V_{GS}=0.5V$ and $V_{DS}=2.5V$. (hint : $I_D=k(V_{GS}-V_{th})^2$ 20%

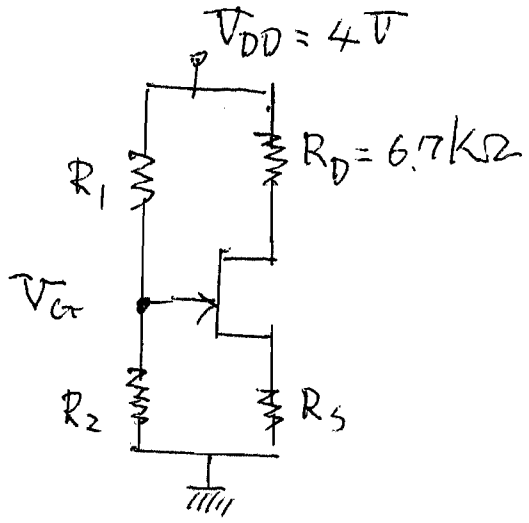

Fig. 4