淡江大學 95 學年度碩士班招生考試試題

14

系別：電機工程學系　　科目：計算機概論(含計算機組織)

准帶項目請打「V」	
	簡單型計算機

本試題共 1 頁

1. Describe briefly the difference between (or among) the follow nouns in computer systems: (20%)
   (a) SISD / MIMD / SIMD
   (b) RISC / CISC
   (c) Temporal locality / Spatial locality
   (d) Write through / Write back
   (e) Assembly program / Microprogram

2. Design a 2×2 switch. The switch has data inputs a and b, a "cross" control signal c, and data outputs x and y. Normal operation of the switch depends on the values of c. When $c=0$, a is connected to x and b to y. When $c=1$, a is connected to y and b to x. (10%)

3. A particular type of Hamming code has 8-bit codeword $P_8D_7D_6D_5P_4D_3P_2P_1$. The parity bits P_i are obtained from the data bits D_j according to logical equation
   $P_1 = D_3 \oplus D_5 \oplus D_6$, $P_2 = D_3 \oplus D_5 \oplus D_7$, $P_4 = D_3 \oplus D_6 \oplus D_7$, $P_8 = D_5 \oplus D_6 \oplus D_7$.
   a) Could this code correct any single-bit error? (Derive the correction rules briefly) (8%)
   b) Could the code detect all double-bit errors in addition to correcting single errors? (7%)

4. An address for a byte-addressable memory presented to the cache unit is divided as follow: 13-bit tag, 14-bit line index, 5-bit byte offset.
   (a) What is the main-memory space in bytes? (3%)
   (b) What is the cache size in bytes? (3%)
   (b) What is the cache mapping scheme? (4%)
   (c) For a given byte in cache, how many different bytes in main memory can occupy it? (5%)

5. A processor chip is used for application in which 30% of execution time is spent on floating-point addition, 25% on floating-point multiplication, and 10% on floating-point division. For the new model of the processor, the design team has come up with three possible enhancements. Which one of these enhancements should be chosen? (20%)
   (a) Redesign the floating-point adder to make it twice as fast.
   (b) Redesign the floating-point multiplier to make it three times as fast.
   (c) Redesign the floating-point divider to make it ten times as fast.

6. The "Superscalar" and "Super-pipelined" approaches are designed to improve the performance of the execution of instructions. (20%)
   (a) Please explain both the operation of "Superscalar" and "Super-pipelined".
   (b) List at least 5 limitations in superscalar machines, describe each briefly.