1. (1) Explain the basic instruction execution cycle of a computer. (5%)
   (2) In the context of pipelining, describe briefly two techniques that can be used to maintain the pipeline when branch instructions are encountered in the instruction stream. (6%)

2. A virtual memory system has a page size of 1024 words, eight virtual pages, and four physical page frames. The machine is word-addressable. The page table is as follows:

Virtual Page Number	Page Frame Number
0	3
1	1
2	–
3	–
4	2
5	–
6	0
7	–

   What are the main memory addresses for the following virtual addresses: 0, 3728, 1023, 1024, 1025, 7800, 4096? (14%)

3. A computer consists of a CPU and an I/O device D connected to main memory M via a 1-word shared bus. The CPU can execute a maximum of 10^5 instructions per second. An average instruction requires five machine cycles, three of which use the memory bus. A memory read or write operation uses one machine cycle. Suppose that the CPU is continuously executing "back-ground" programs that requires 95% of its instruction execution rate but not any I/O instructions. Now the I/O device is to be used to transfer very large blocks of data to and from main memory M.
   (1) If programmed I/O is used and each 1-word I/O transfer requires the CPU to execute two instructions, estimate the maximum I/O data transfer rate γ_{MAX} possible through D. (6%)
   (2) Estimate γ_{MAX} if DMA (Direct Memory Access) is used. (6%)

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4. Create the state table and draw the state diagram for
   (1) a D flip-flop **(4%)**
   (2) a T flip-flop **(4%)**
   (3) a SR flip-flop (include a third state, U, for the state in which the output is undefined). **(6%)**

5. (1) Consider an n-stage pipeline where each stage requires 1 time unit to process a subtask, and tasks are delivered to the pipeline at the rate of one every 1 time unit. Compute the maximum throughput of this pipeline for an input stream of k tasks. **(6%)**
   (2) What is the speedup of such a pipeline relative to a non-pipelined system that also processes k tasks? **(6%)**

6. Show the representation of the following values in signed-magnitude notation and signed-two's complement notation. Including the sign bit, each number has a total of 8 bits.
   (1) –63　　**(4%)**　　(2) 147　　**(4%)**　　(3) 85　　**(4%)**

7. Let a be an array of integers. Present recursive algorithms to compute:
   (1) The maximum element of the array **(6%)**
   (2) The sum of the elements of the array **(6%)**

8. In a hypothetical computer, assume that the normalized floating point value format in hexadecimal is used, which is written as

$$x = (0.abbbbb)_{16} \times 16^k$$

where a is a non-zero hexadecimal digit and b's are hexadecimal digits including zero; k is an exponent and expressed in binary. The mantissa has 6 hexadecimal digits. In this computer, a single precision floating point value uses 32 bits, among which the first bit records the sign of mantissa, the next 7 bits are for the exponent, and the last 24 bits are for the mantissa. The exponent is biased by $(64)_{10}$ and stored in the 7 bits. Find
   (1) the smallest and largest floating numbers **(8%)**
   (2) the second smallest floating number **(5%)**