淡江大學八十七學年度碩士班入學考試試題

系別： 電機工程學系　　科目： 計算機概論(含計算機組織)

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1. (20 points) Explain the following terminologies :
   (1) Hash
   (2) Cycle Stealing
   (3) MIN (Multistage interconnection networks)
   (4) ATM (Asynchronous Transfer Mode) Network
   (5) FPGA

2. (10 points) Most computers use interleaved memory. Describe what this means and give an illustrated example. How does interleaving strategy affect memory system throughput and latency ?

3. (10 points) Write a recursive function for computing the binomial coefficient C(n,m) as defined as follows :
   $C(n,m) = (n!) / (m! \times (n-m)!)$ or $C(n,m) = C(n-1, m) + C(n-1, m-1)$
   where $C(n,0) = C(n,n) = 1$.

4. (10 points) Design a 3-bit odd parity generator (the inputs are *a,b,c* and the output is *P*) and a 4-bit odd parity checker. (The inputs are *a,b,c,P* and the output is *C*. When error is detected, *C=1*; otherwise *C=0*.)

5. (10 points) From the architecture point of view, what techniques can be used to make a computer run faster ? (for example, computer with cache memory will run faster than the one without cache does) List as many as you can explanation.

6. (10 points) To provide cache consistency in computer, the data cache supports a protocol known as MESI (Modified/Exclusive/Shared/Invalid) protocol. Describe what is the write once policy in the MESI protocol.

7. (10 points) Give reasons that the page size in a virtual memory system should be neither very small nor very large.

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8. (10 points)
   (a) Please use transmission gates and inverters directly to implement an 4-to-1 multiplexer.
   (b) Use transmission gates and inverters to implement an 8-to-1 multiplexer which must consist of 4-to-1 and 2-to-1 multiplexers.

9. (10 points) To design a finite state machine we can follow the following steps:
   (A) Understand the problem.
   (B) Obtain an abstract representation of the FSM (such as draw the state diagram or ASM chart to make the state table).
   (C) Perform state minimization.
   (D) Perform state assignment.
   (E) Choose flip-flop types for implementing the FSM's state.
   (F) Implement the finite state machine.

   Now follow the steps as mentioned to design and implement a code converter. The code converter can be specified as the following state tables.

abcd	a'b'c'd'
0000	0 1 1 0
0001	0 1 1 1
0010	1 0 0 0
0011	1 0 0 1
0100	1 0 1 0
0101	1 0 1 1
0110	1 1 0 0
0111	1 1 0 1
1000	1 1 1 0
1001	1 1 1 1

Use JK flip-flops to implement this code converter.