淡江大學八十八學年度碩士班招生考試試題

系別：電機工程學系　　科目：電子學　　本試題共 3 頁　P1

1. Fig.1 shows a three-stage amplifier in which the stages are directly coupled. The amplifier, however, utilizes bypass capacitors, and, as such, its frequency response falls off at low frequencies. For our purpose here, we shall assume that the capacitors are sufficiently large to act as perfect short circuits at all signal frequencies of interest. Assume $|V_{BE}| = 0.7$ V , $\beta = 100$, and neglect the Early effect.
(a) 4% Find the input resistance and the output resistance.
(b) 4% Find the voltage gain *vo/vi*.

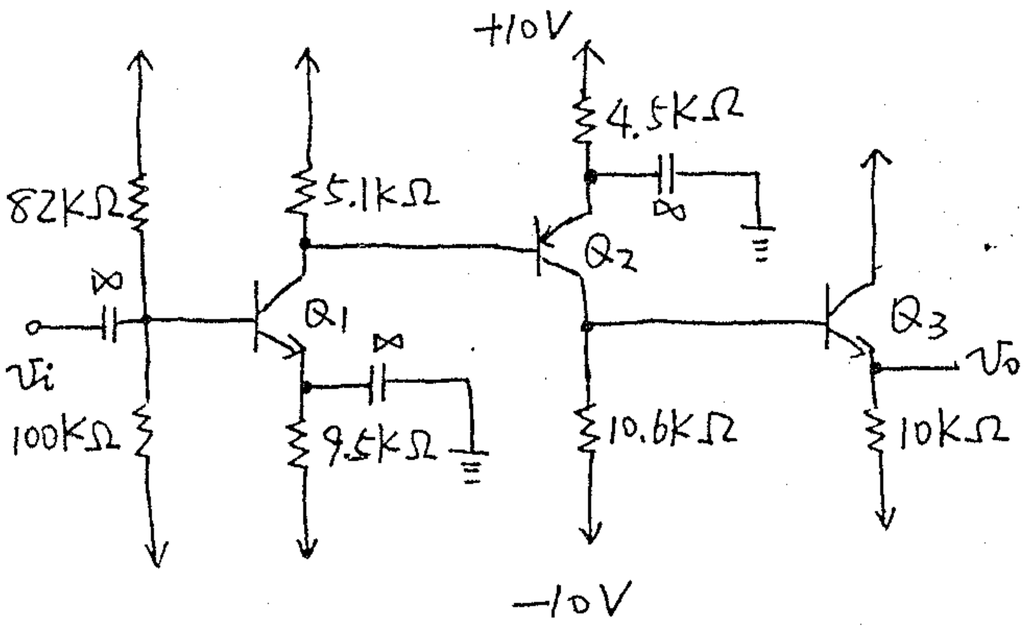

Fig. 1

2. In the CMOS op amp shown in Fig.2 , all MOS devices have $|V_t| = 1$V , $\mu nCox = 2\mu pCox = 40\mu A/V^2$, $|V_A| = 50$V, and L = 5μm. Device widths are indicated on the diagram as multiples of W , where W = 5 μm.
(a) 4% Design R to provide a 10-μA reference current.
(b) 4% Assuming $vo = 0$V , as established by external feedback, perform a bias analysis , finding Vc=?

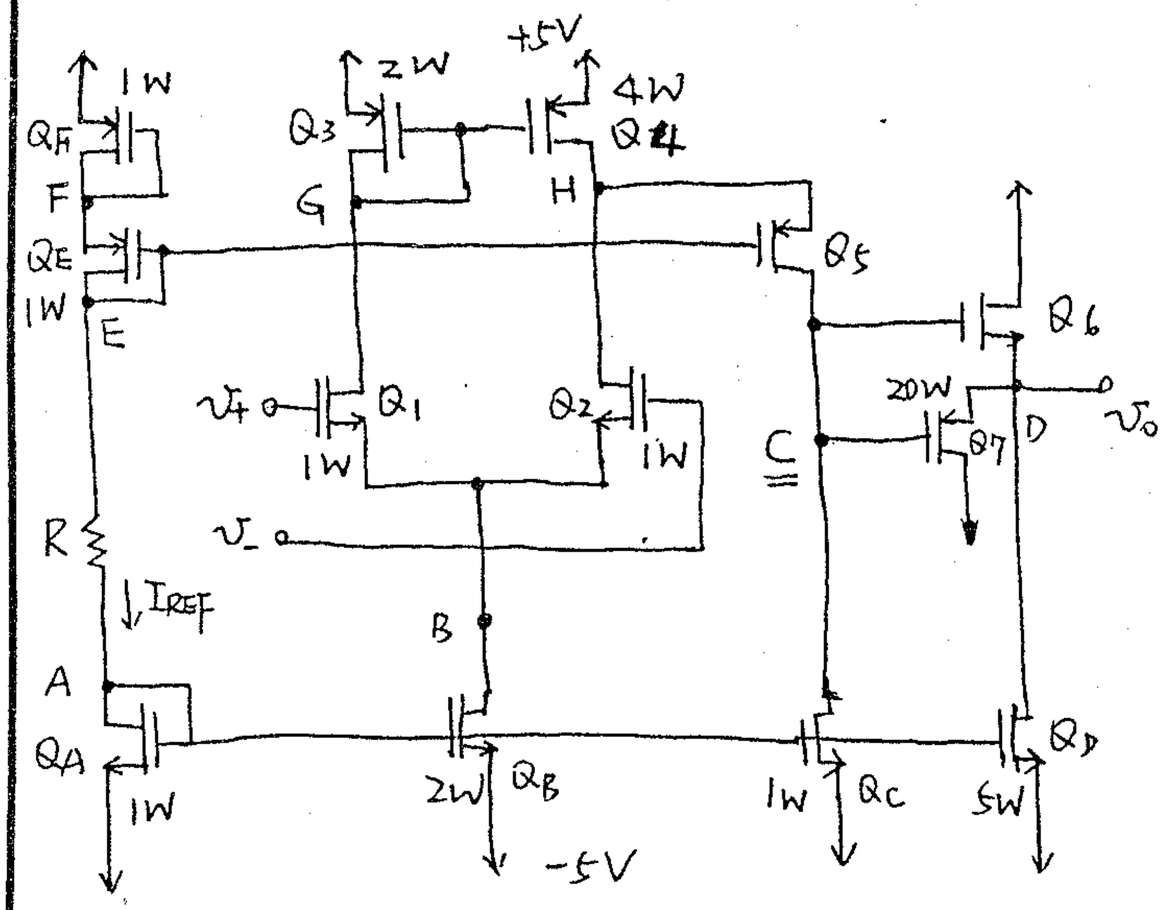

Fig. 2

3. 8% For the amplifier circuit in Fig.3 , assuming that Vs has a zero dc component. Let the BJTs have β = 100. Use feedback analysis to find Vo/Vs and Rin.

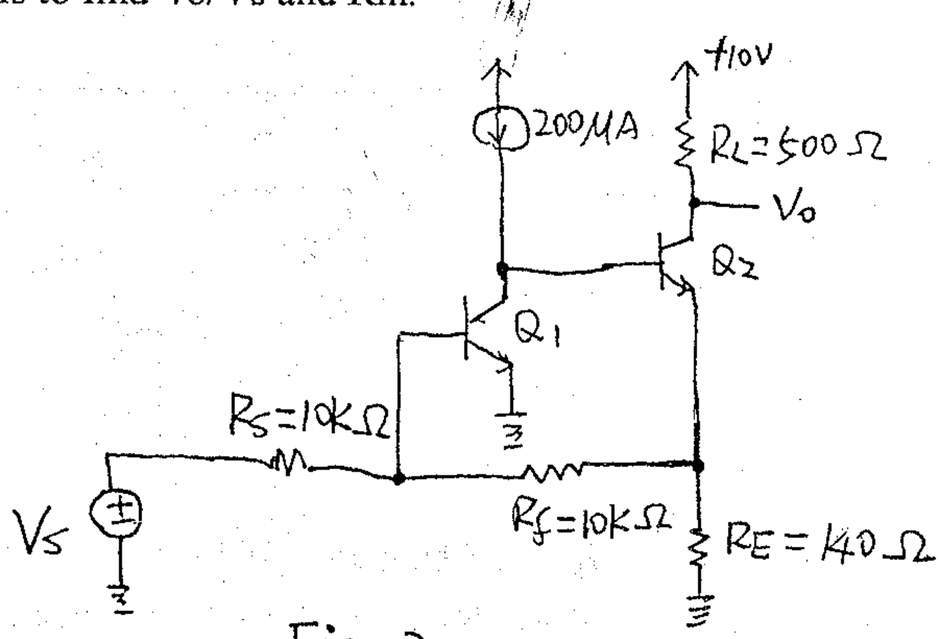

Fig. 3.

4. 8% An op amp with an open-loop voltage gain of 80 dB and poles at 10^5 , 10^6 , and 2×10^6 Hz is to be compensated to be stable for unity β. Assume that the op amp incorporates an amplifier equivalent to that in Fig.4 , with C1 = 150pF, C2 = 5pF, and gm = 40mA/V, and that f_{P1} is caused by the input circuit and f_{P2} by the output circuit of this amplifier. Find the required value of the compensating Miller capacitance and the new frequency of the output pole.

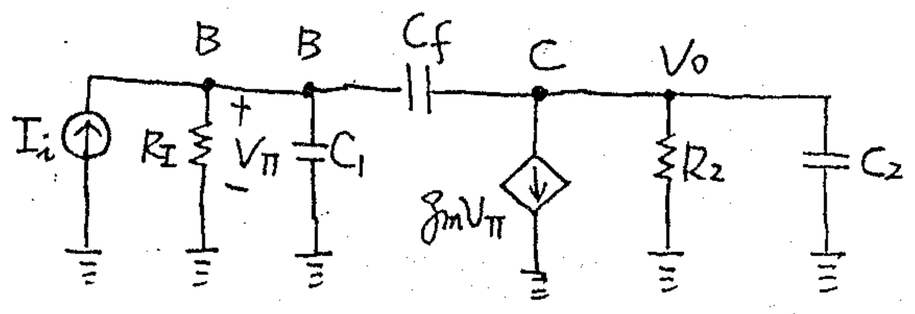

Fig. 4.

5. 8% The BJTs in the circuit of Fig.5 have βP = 10, βN=100, $|V_{BE}| = 0.7$V, $|V_A| = 100$V. Find the values of Vo/Vi and Rin.

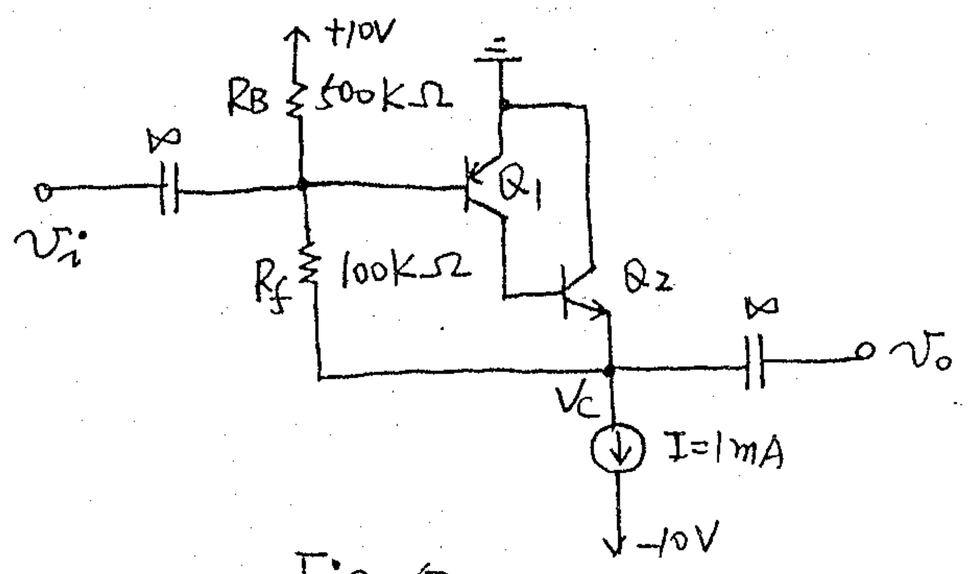

Fig. 5.

1. 答案請標示清楚。
2. 請按題序作答，先寫會作的。

注意背面尚有試題

6. 8% For the circuit in Fig.6, break the loop at node X and find the loop gain (working backward for simplicity to find Vx in terms of Vo). For R = 10kΩ, find C and R_f to obtain sinusoidal oscillations at 10kHz.

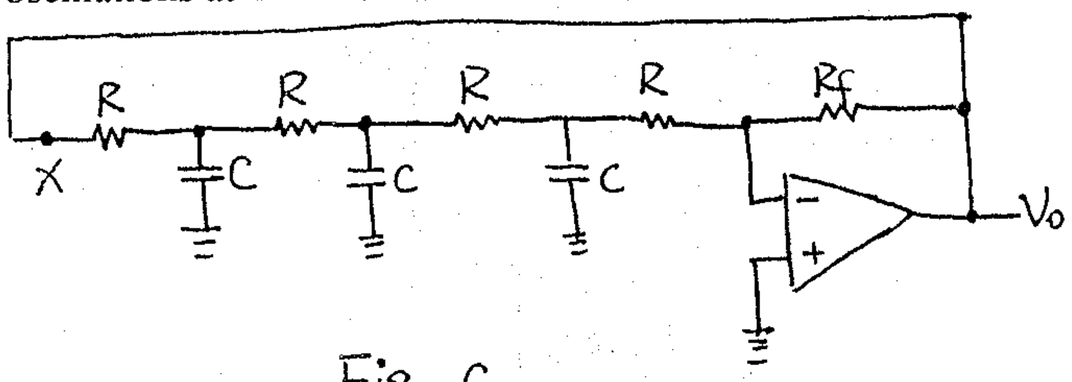

Fig. 6.

7. 4% A CMOS inverter for which kn = 10kp = 100μA/V² and Vt = 0.5V is connected as shown in Fig.7 to a sinusoidal signal source having a Thevenin equivalent voltage of 0.1-V peak amplitude and resistance of 100 kΩ. What signal voltage appears at node A with VI = +1.5V?

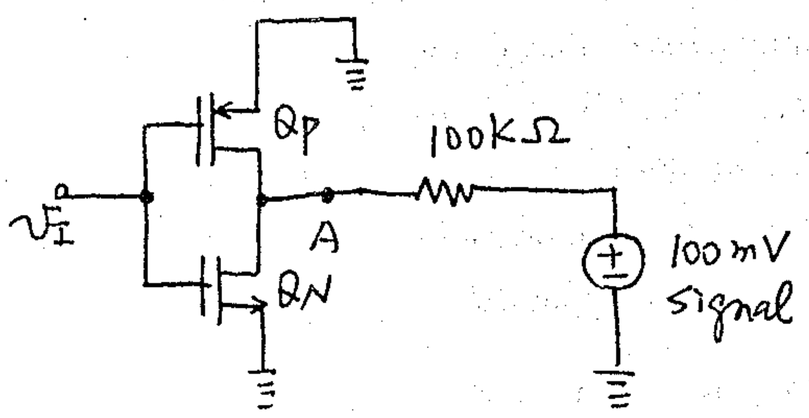

Fig. 7.

8. 8% If Vγ = 0.7V for the diode in the circuit shown in Fig.8 , determine I_D and Vo .

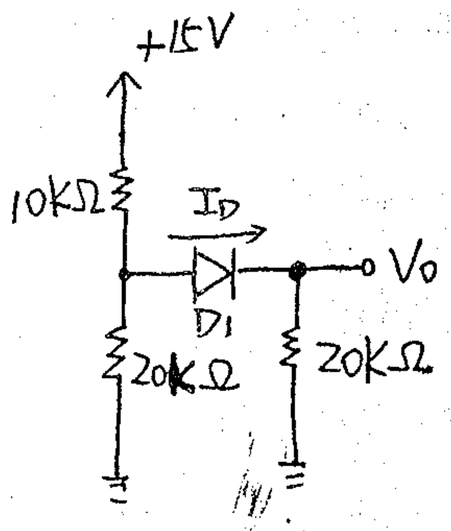

Fig. 8.

9. 8% For the circuit shown in Fig.9 , let β = 125. Find I_{CQ} and V_{CEQ}.

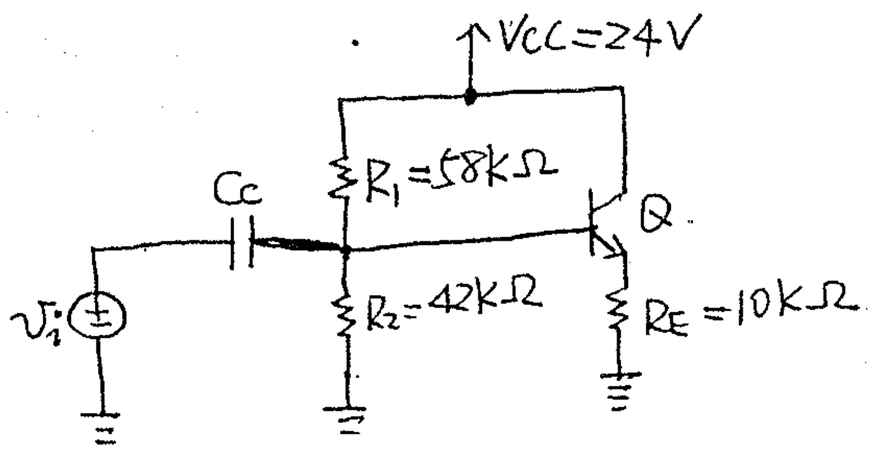

Fig. 9.

10. 12% The parameters for each transistor in the circuit shown in Fig.10 are: β = 80 , and V_{BE}(on) = 0.7 V . Determine the quiescent values of base, collector, and emitter currents in Q_1 and Q_2.

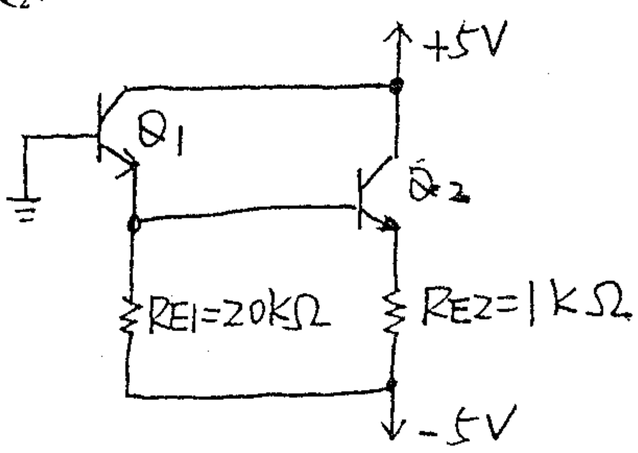

Fig. 10.

11. 8% The transistors shown in the circuit in Fig.11 both have parameters V_{Th} = 0.8 V and $(^1/_2)\mu_n Cox$ = 15 μA/V² . If the width-to-length ratios of M_1 and M_2 are $(W/L)_1 = (W/L)_2 = 40$, determine V_{GS1}, V_{GS2}, Vo, and I_D.

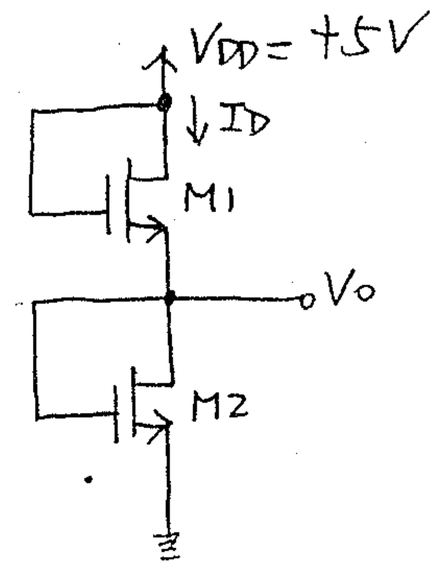

Fig. 11

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12. 4% Determine the logic function implemented by the circuit shown in Fig.12 .

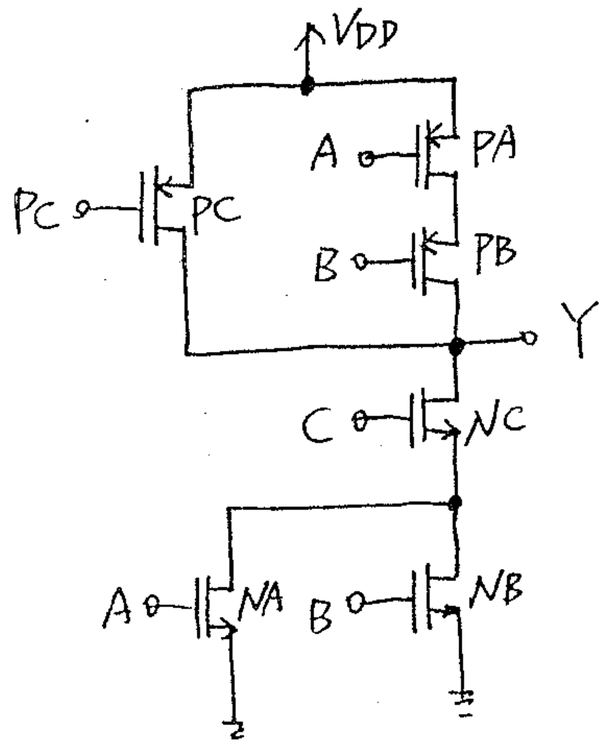

Fig. 12:

13. 4% What is the logic function implemented by the circuit shown in Fig.13 ?

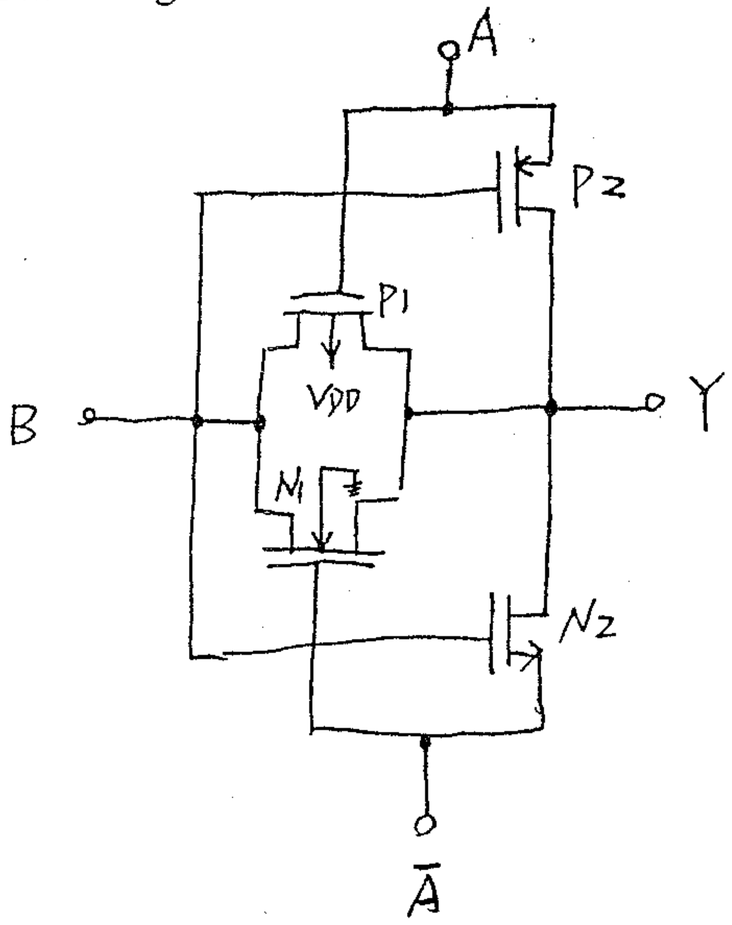

Fig. 13

14. 4% The op-amp in the circuit shown in Fig.14 has an open-loop differential voltage gain of $A_d = 10^4$. Neglect the current into the op-amp , and assume the output resistance looking back into the op-amp is zero . Determine the closed-loop voltage gain Av = Vo/Vs.

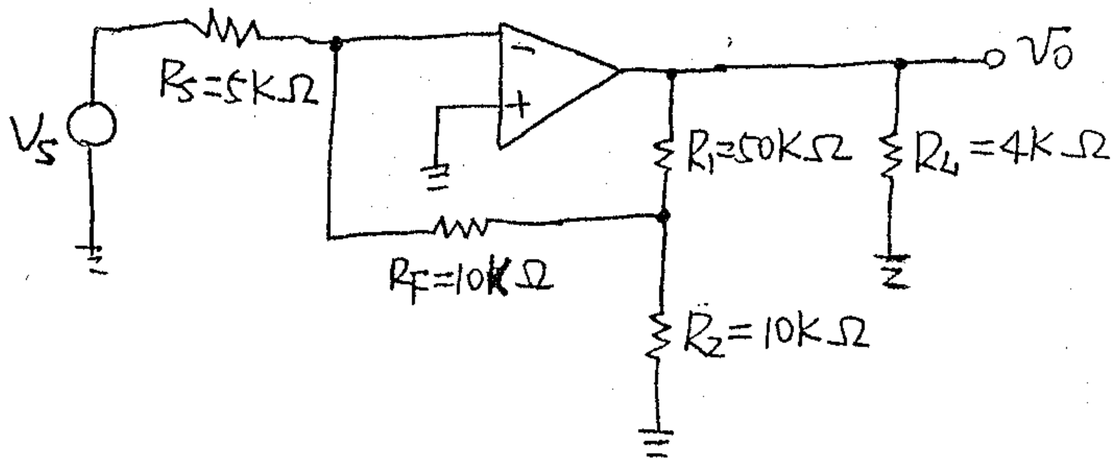

Fig. 14.

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