

# 淡江大學八十七學年度碩士班入學考試試題

系別： 電機工程學系

科目： 電子學

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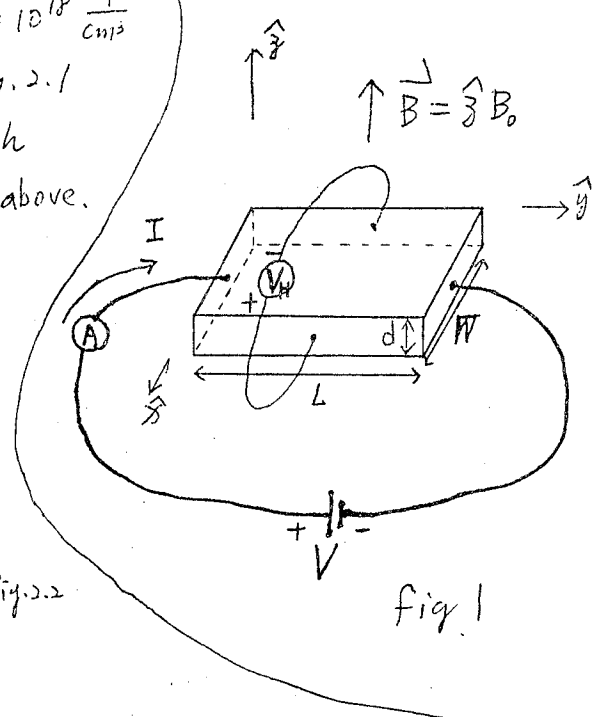
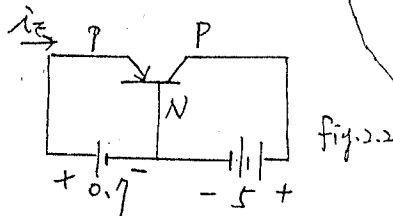
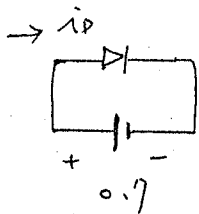
(一) (a) what is the semiconductor type in the right figure. (b) If the 10% semiconductor is uniformly doped, what is the majority carrier concentration (in terms of the measured  $B_0$ ,  $V_H$ , etc.)

(二) A PN junction is formed with  $N_A = 10^{18} \frac{1}{cm^3}$  and  $N_D = 10^{15} \frac{1}{cm^3}$ . The diode of fig. 2.1 and EBJ of fig. 2.2 are made with the same PN junction mentioned above.

(a) choose one answer below

①  $i_D > i_E$    ②  $i_D = i_E$    ③  $i_D < i_E$

(b) Explain your choice



(三) One of the Ebers-Moll model of a BJT is given by

$$i_D = -\alpha_F i_E - I_{C0} \left( e^{\frac{V_{BC}}{V_T}} - 1 \right) \dots \textcircled{1}$$

$$i_E = -I_{E0} \left( e^{\frac{V_{BE}}{V_T}} - 1 \right) - \alpha_R i_D \dots \textcircled{2}$$

The advantage of EM model is that  $\alpha_F$ ,  $\alpha_R$ ,  $I_{E0}$  and  $I_{C0}$  can be measured directly by experiment.

(a) Write down suitable expressions for  $\alpha_F$ ,  $\alpha_R$ ,  $I_{E0}$  and  $I_{C0}$  in terms of the terminal voltages and currents, respectively.

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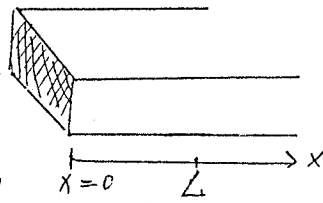
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(b) According to your expressions in part (a), set up some experiments to measure  $\alpha_F$ ,  $\alpha_R$ ,  $I_{E0}$  and  $I_{C0}$ , respectively.

(IV) (a) An infinite-plane perfume source with constant concentration  $P_0$  is located



at  $x=0$ . At  $t=0$ , the concentration  $P(x)=0$ , for  $x>0$  (in air). What will be the concentration  $P_L = P(x)|_{x=L}$  as  $t \rightarrow \infty$ ?

(b) If the plane perfume source is replaced with a hole source with constant concentration  $P_0 \gg P_{n0}$ , where  $P_{n0}$  is the hole concentration of a doped n-semiconductor at  $x>0$  and  $t=0$ .

What will be the concentration  $P_L = P(x)|_{x=L}$  as  $t \rightarrow \infty$ ?

(Assume  $L = L_p$ , the diffusion length of hole)

(c) Which one is bigger comparing  $P_L$  and  $P_L$ ? why?

(V) Assume an NMOS FET is in triode region for a specified  $V_{GS}$ , of which the drain current  $i_D$  increases as  $V_{DS}$  increases.

How does the channel resistance  $\frac{V_{DS}}{i_D}$  change as  $V_{DS}$  increases?

(increase, decrease or unchange)

Give your explanation!

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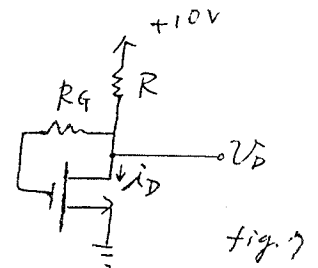
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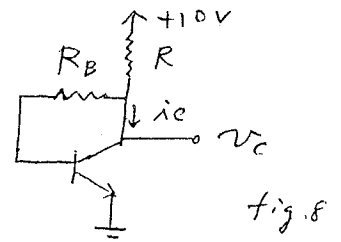
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(六) Consider the channel depth of an enhanced NMOS ( $V_t = 1$  volt) 10% and a depletion NMOS ( $V_t = -1$  volt).  
when  $V_{GS} = 2, 0$  and  $-2$  volt, respectively,  
which MOS has deeper channel?

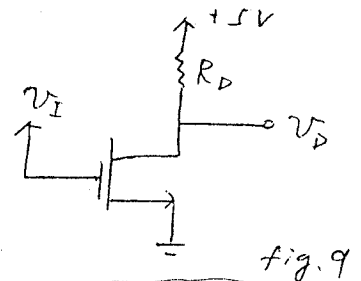
(七) Let  $R = 15\text{K}\Omega$ ,  $R_G = 0\text{K}$ , find  $i_D$ ,  $V_D$ !  
10% (NMOS:  $V_t = 2\text{V}$ ,  $K = 0.1\text{ mA/V}^2$ )



(八) Let  $R = 15\text{K}$ ,  $R_B = 0\text{K}$ , find  $i_C$ ,  $V_C$ !  
10% ( $\beta = 100$ )



(九) Fig. 9 is an inverter. (a) Design  $R_D$  such that 10%  $V_O = 0.1$  volt when  $V_I = 5$  volt.  
(NMOS:  $V_t = 1$  volt and  $K = 0.5\text{ mA/V}^2$ )  
(b) what is the turn on resistance?



(十) In fig. 10, if  $V_G$  is set at 3 different voltages 10% 0 volt, 2 volt and 10 volt, respectively,  
the MOSFET is in which region  
(triode, Pinch-off, cut-off)?  
(Assume NMOS:  $V_t = 1$  volt,  $K = 0.5\text{ mA/V}^2$ )

