沙江大學九十四學年度碩士班招生考試試題 104-1

系別:資訊工程學系 科目:計算機組織與系統(含作業系統、計算機組織)

准帶項目請打「V」
簡單型計算機
本試題共 2 頁

- 1 Explain the following terms as details as possible (10%)
- (a) Thrashing (b)Belady's anomaly (c)DMA (d)RAID (e)RISC

2. Consider the following snapshot of a system.

B. bha saidibhean eire

医复数形式多种

(With Exitation in Allocation 137 Max Available В \boldsymbol{C} C \boldsymbol{c} D 0 2 5 2 0 0 0 1 2 0 1 0 5 3 4 2 3 5 6 5 2 0 6 3 2 0 6 0 0

- (a) What is the content of the matrix Need? (5%)
- (b) List the safe sequence if it exists. (10%)
- (c) If a request from process P_1 arrives for (0,4,2,0), can the request be granted immediately? Explain the reason of your answer. (5%)
- 3. (a) List the information stored in PCB. Describe the actions taken by a kernel to context switch. (10%)
 - (b) Draw the process state transition diagram. Explain why a context switch may happen. (10%)
- 4. Draw a diagram to show the translation from logical address to physical address under single-level paging system with TLB. (10%)

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- 5. Consider a two-level memory hierarchy, M_1 and M_2 . Denote the hit ratio of M_1 as h. Let C_1 and C_2 be the costs per kilobyte, S_1 and S_2 the memory capacities, and T_1 and T_2 the access times, respectively.
- (a) What is the effective memory-access time T_a of this hierarchy? (5%)
- (b) Let $r = T_2/T_1$ be the speed ratio of the two memories. Let $E = T_1/T_a$ be the access efficiency of the memory system. Express E in terms of r and h. (5%)
- 6. Use NAND gate to implement AND, OR, and NOT gates. (15%)
- 7. (a) What is the IEEE 754 representation of 32-bit integer binary format of a signed decimal number, -300? (7%)
 - (b) What is the IEEE 754 representation of 32 bits floating point binary format of a signed decimal number, -29.75? (8%)