淡江大學八十九學年度日間部轉學生招生考試試題

46

系別：電機工程學系三年級　　科目：電 子 學

本試題共 2 頁

本試題雙面印製

(一) Find the input impedance $R_{in}\left(=\frac{V_i}{I_i}\right)$ for the circuit shown below

20%

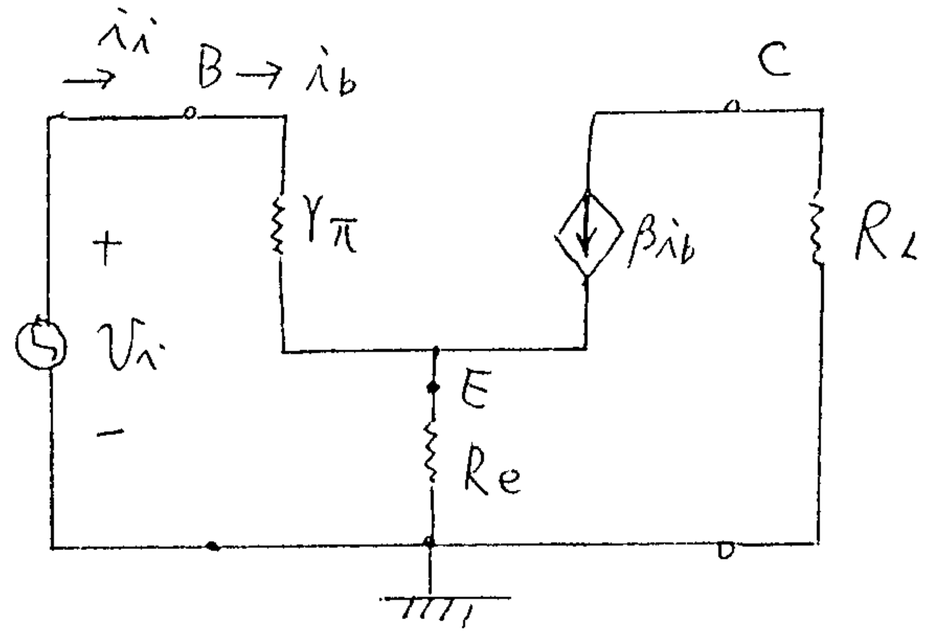

fig. 1

(二) For the circuit of fig. 2, determine V_o in terms of V_1, V_2, and V_3 (assume the OpAmp is ideal)

20%

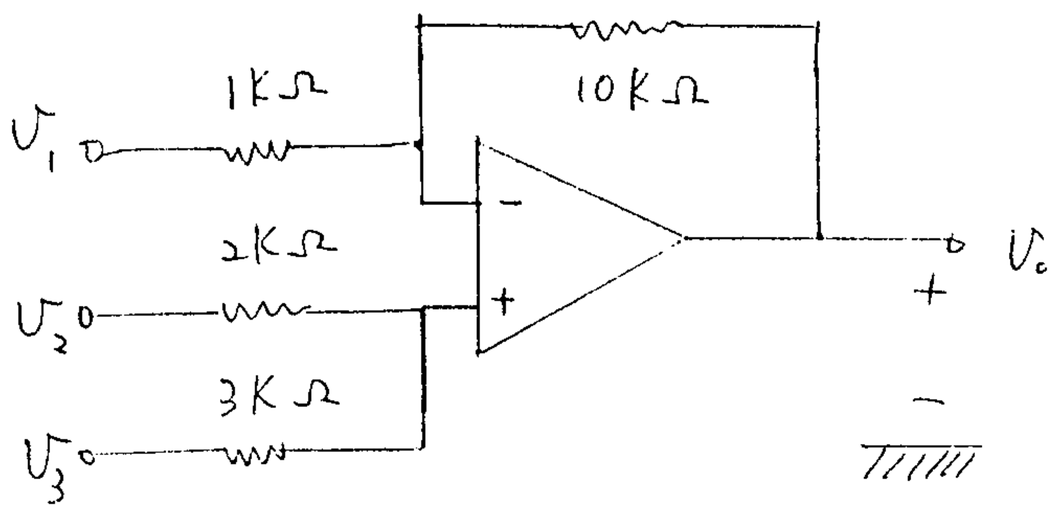

fig 2.

(三) The zener diode in the shunt regulator of fig. 3 has incremental resistance

20%

7Ω. Also, the break down voltage is 5.1 volt at a current of 50mA. Find the output voltage at no load, the line regulation and the load regulation.

fig. 3

注意背面尚有試題▶

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(四) In fig. 4, the β is in the range of 50 to 150, design a suitable 20% R_C such that all fabricated circuits are all in the active mode.

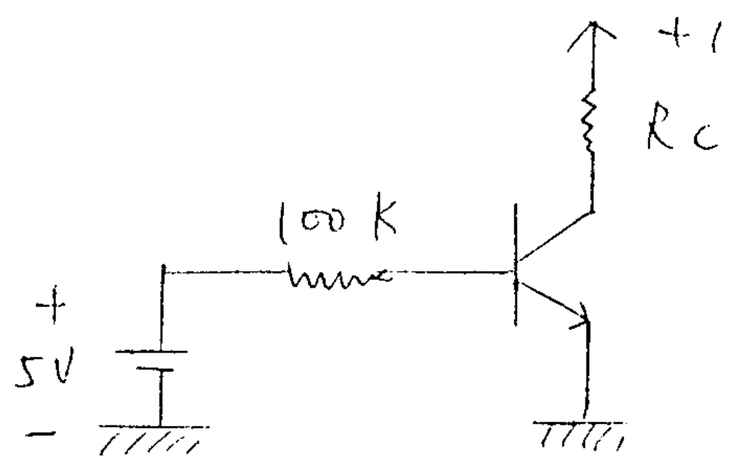

fig. 4

(五) An enhancement - type NMOS transistor has threshold voltage 20% $V_t = 2$ volt. It conducts a current $i_D = 1mA$ when $V_{GS} = V_{DS} = 3$ volt. Find the value of i_D when $V_{GS} = 4$ volt and $V_{DS} = 5$ volt. (Neglecting the channel length modulation effect)